

CLAIMS:

What is claimed:

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1 1. An integrated circuit comprising:
2 a first port for outputting a signal;
3 a second port for receiving said signal;
4 an alignment link for electrically connecting said first port with said second port;
5 and
6 said alignment link comprises a signal buffer for buffering a signal traveling along
7 said alignment link between said first port and said second port.

1 2. An integrated circuit according to claim 1 wherein said alignment link
2 further comprise a wiring trace.

1 3. An integrated circuit according to claim 1 wherein said alignment link
2 comprises a common area of integrated circuit real estate.

1 4. An integrated circuit according to claim 1 wherein said first port is located
2 in a first area of integrated circuit real estate.

1 5. An integrated circuit according to claim 1 wherein said second port is
2 located in a second area of integrated circuit real estate.

1 6. ~~An integrated circuit according to claim 1 wherein said integrated circuit~~
2 ~~real estate comprises multi-levels.~~

1 7. An integrated circuit according to claim 6 wherein said multi-levels
2 comprise a semiconductor level and a wire tracing level.

1 8. An integrated circuit according to claim 7 wherein said semiconductor
2 level comprises said signal buffer.

1 9. An integrated circuit according to claim 7 wherein said wire-tracing level
2 comprises said first port and said second port.

1 10. ~~An integrated circuit according to claim 9 wherein said wire-tracing level~~
2 ~~comprises a plurality of levels.~~

1 11. A method of aligning ports in an integrated circuit comprising the steps of:
2 extending a first port from one area into a common area;
3 extending a second port from a second area into said common area; and
4 linking said first port to said second port within said common area via an
5 alignment link wherein said alignment link comprises a wiring trace and a signal buffer.

1 12. A method of aligning ports in an integrated circuit according to claim 11
2 wherein said common area comprises a multi level area.

1 13. A method of aligning ports in an integrated circuit according to claim 12
2 wherein said multi-level area comprises a wiring level and a semiconductor level.

1 14. A method of aligning ports in an integrated circuit according to claim 13
2 wherein said semiconductor level comprises said signal buffer.

1 15. A method of aligning ports in an integrated circuit according to claim 13
2 wherein said wiring level comprises said wiring trace.

1 16. A method of aligning ports in an integrated circuit according to claim 11
2 wherein said first area and said second area are at a substantial distance from each other
3 relative to overall integrated circuit real estate.

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1 17. An integrated circuit comprising :
2 a first port for outputting a signal;
3 a second port for receiving said signal; and
4 an alignment means for electrically connecting said first port with said second
5 port.

1 18. An integrated circuit according to claim 17 wherein said alignment means
2 comprises a wiring trace and signal buffering circuitry.

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1 19. An integrated circuit according to claim 18 wherein said wiring trace and
2 said signal buffering circuitry occupy a common area of integrated circuit real estate.

1 20. An integrated circuit according to claim 19 wherein said first port and said
2 second port are located at a substantial distance to each other relative to overall integrated
3 circuit real estate.

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